B'cont

amplifier including a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate.

14. (once amended) An operational amplifier circuit comprising:

a first NMOS depletion mode amplification stage;

a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage;

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a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and

and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a resistor;

and further wherein said first NMOS depletion mode amplification stage, first NMOS depletion mode chopping switch, second NMOS depletion mode chopping switch, and said NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit are fabricated on the same silicon carbide substrate.

REMARKS

The Office Action mailed October 23, 2002 and the Advisory Action dated February 18, 2003 have been carefully reviewed and the foregoing amendment has been made in consequence thereof. Submitted herewith is a Submission of Marked Up Claims.